

006221" 20815460

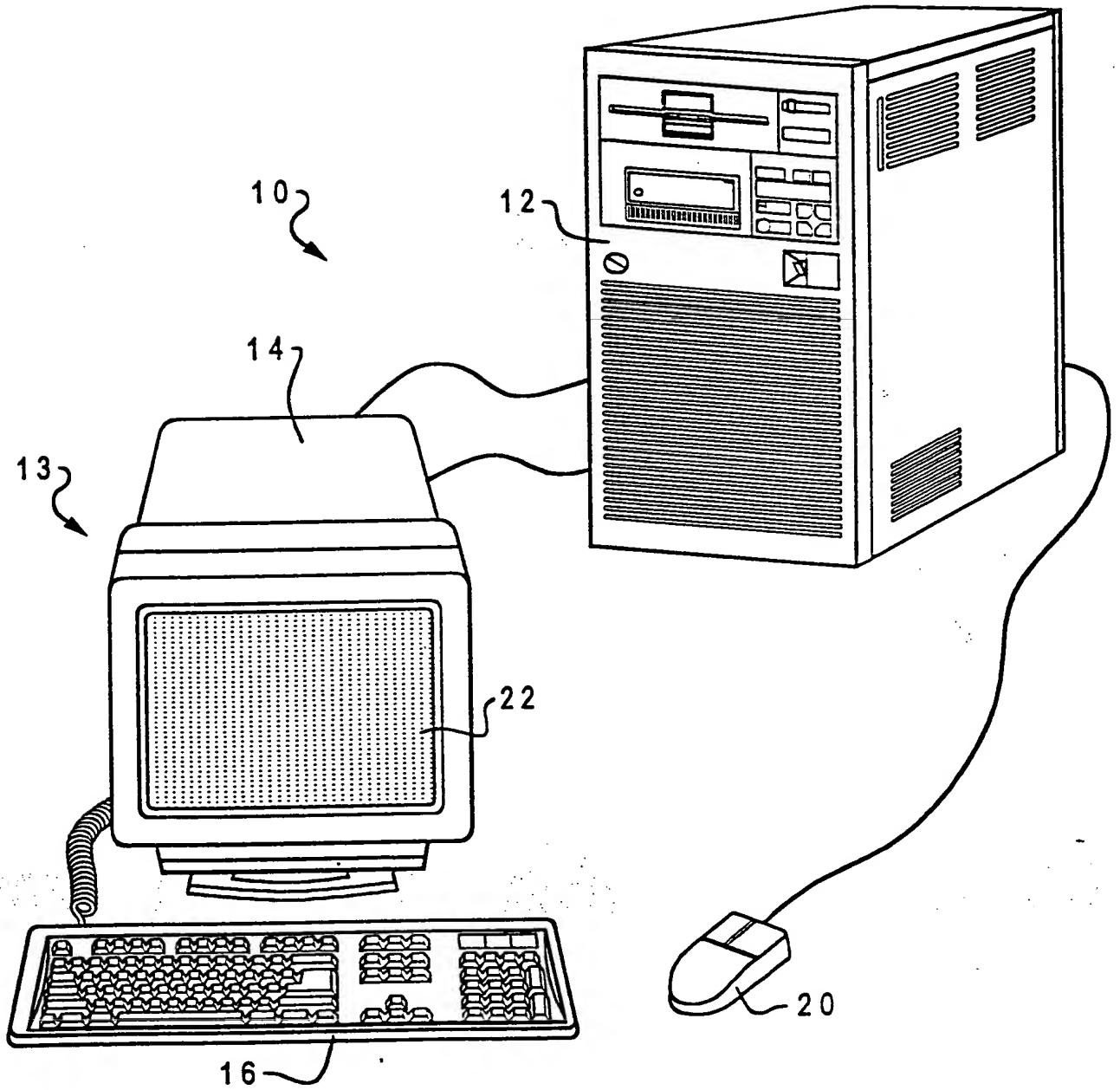


Fig. 1

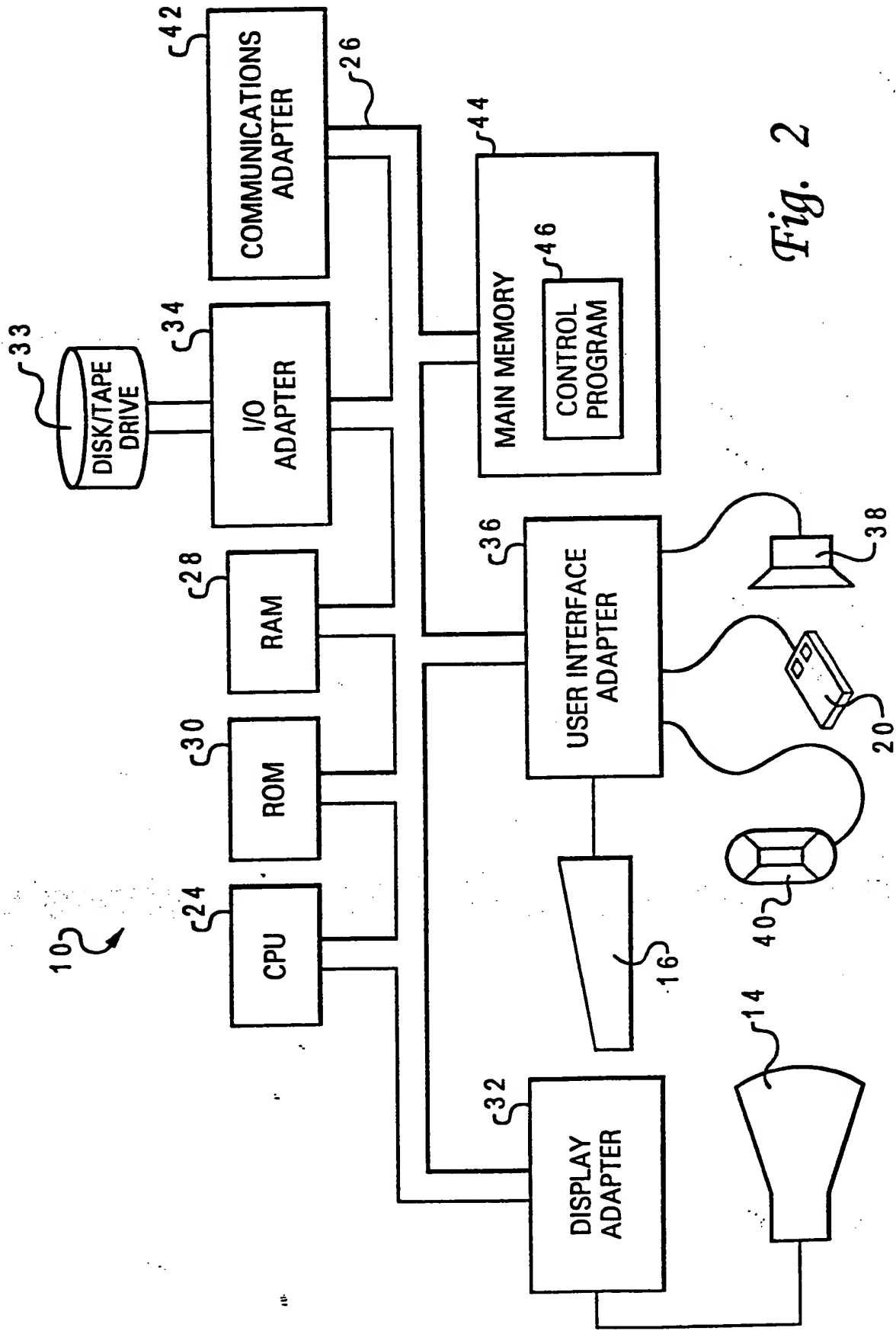


Fig. 2

006227 208T5260

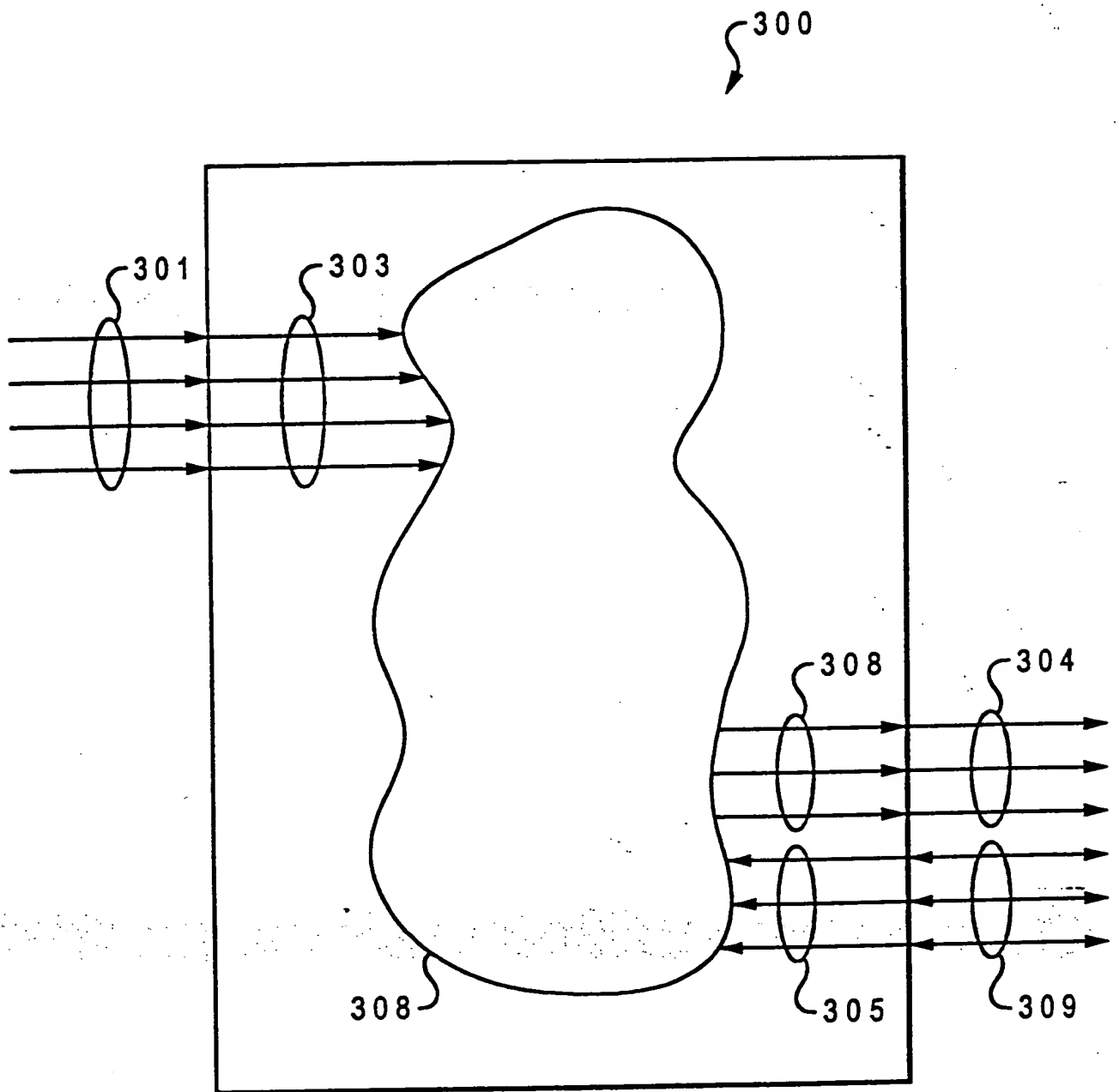


Fig. 3A

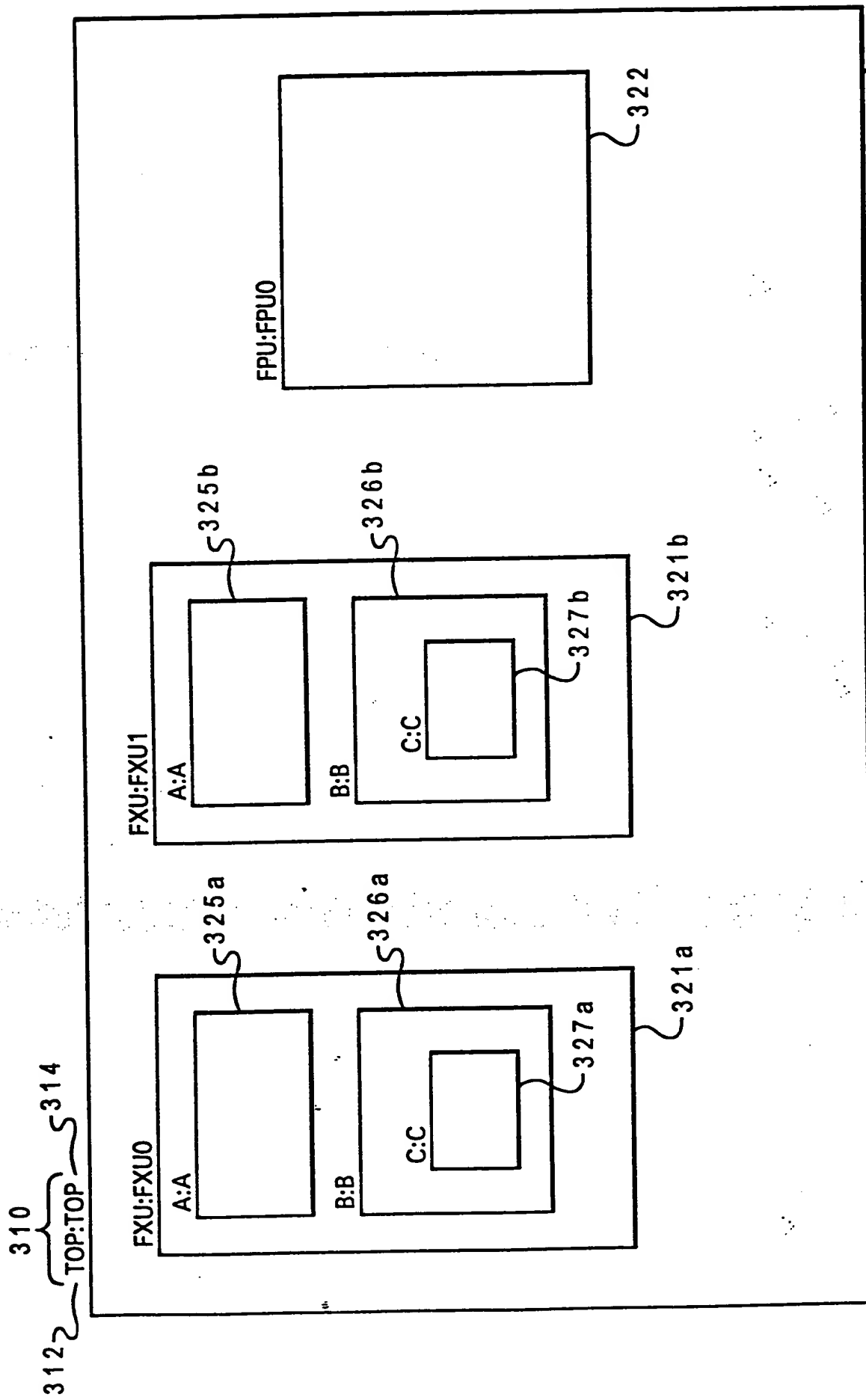


Fig. 3B

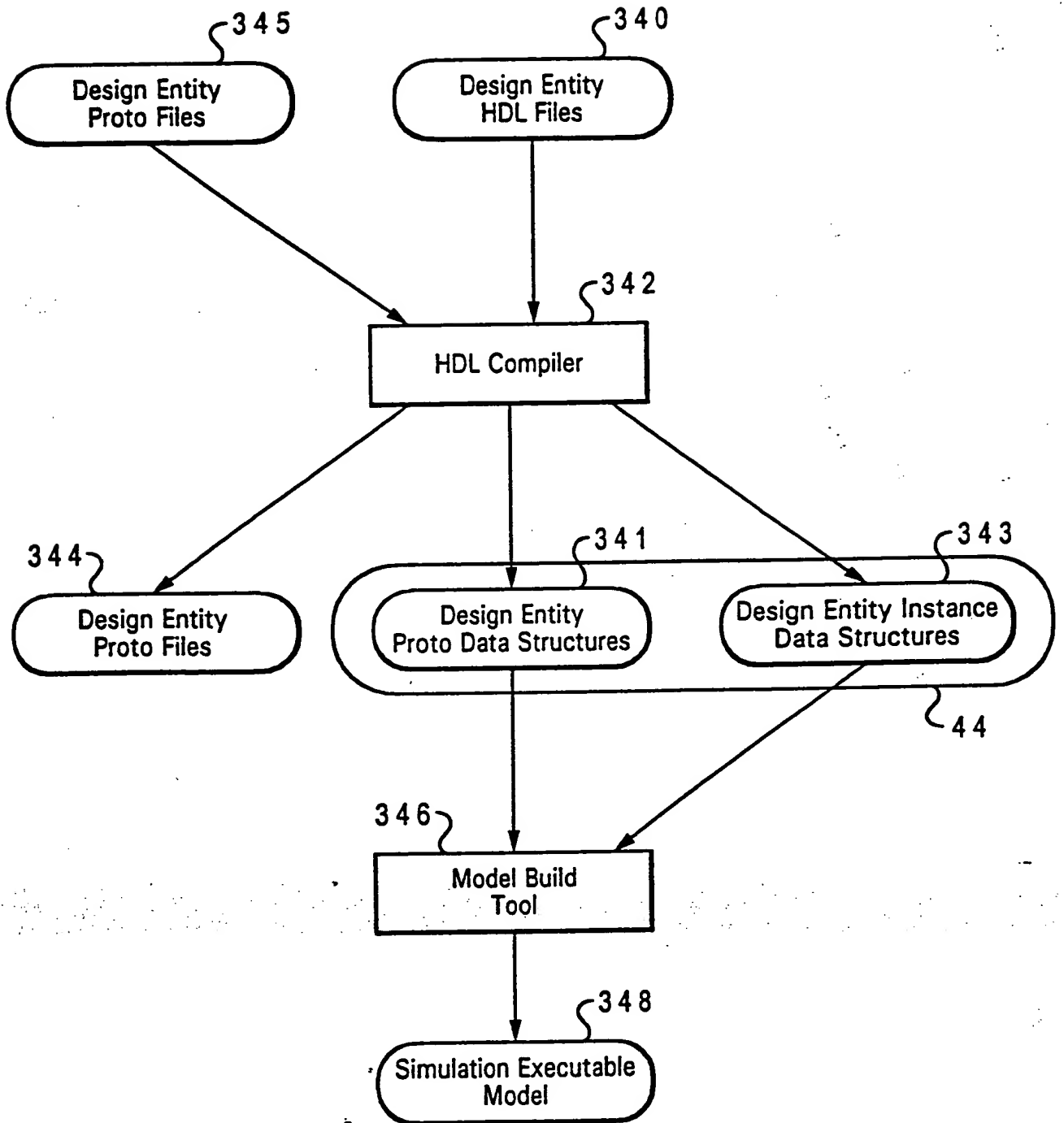


Fig. 3C

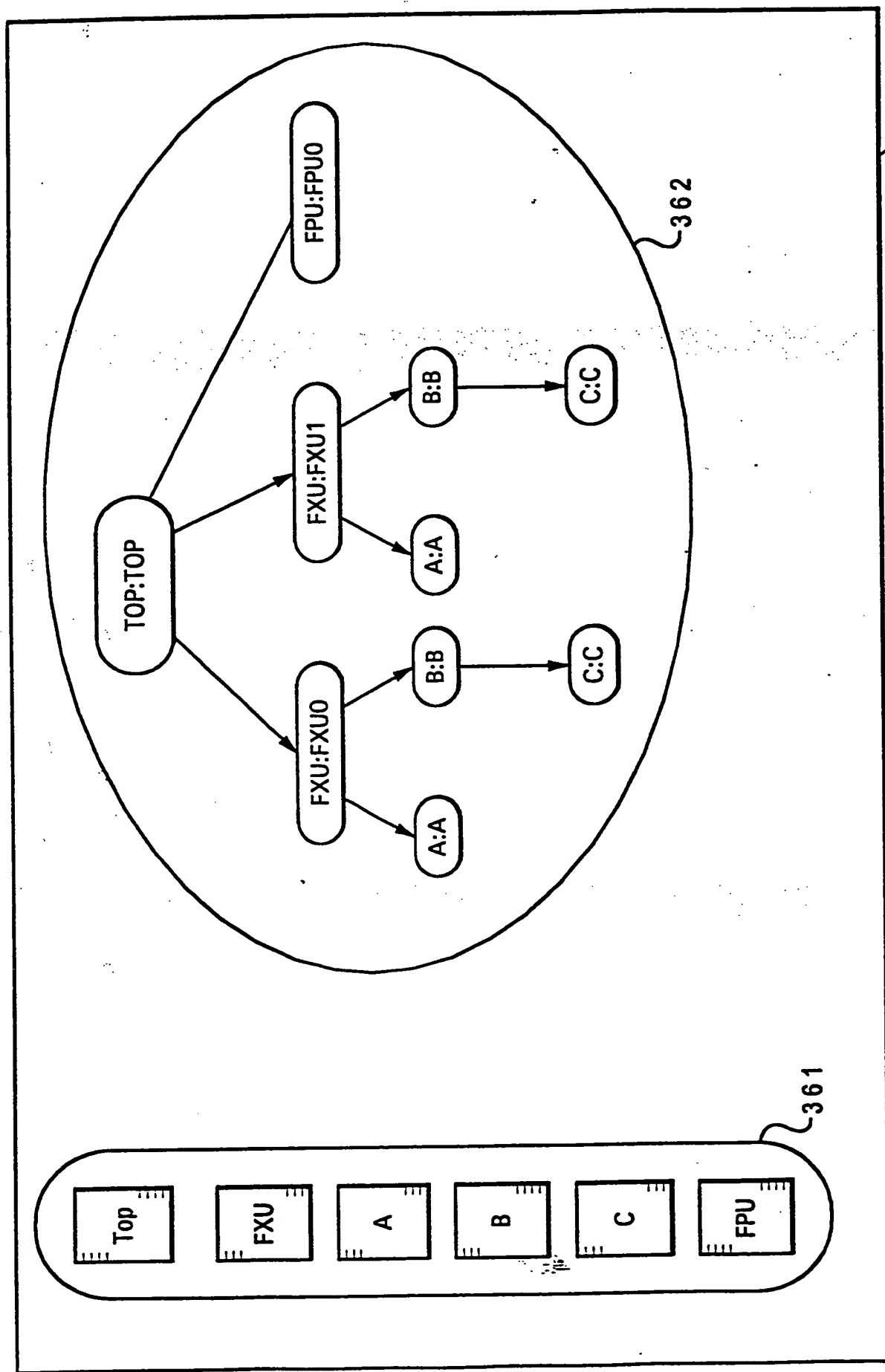


Fig. 3D

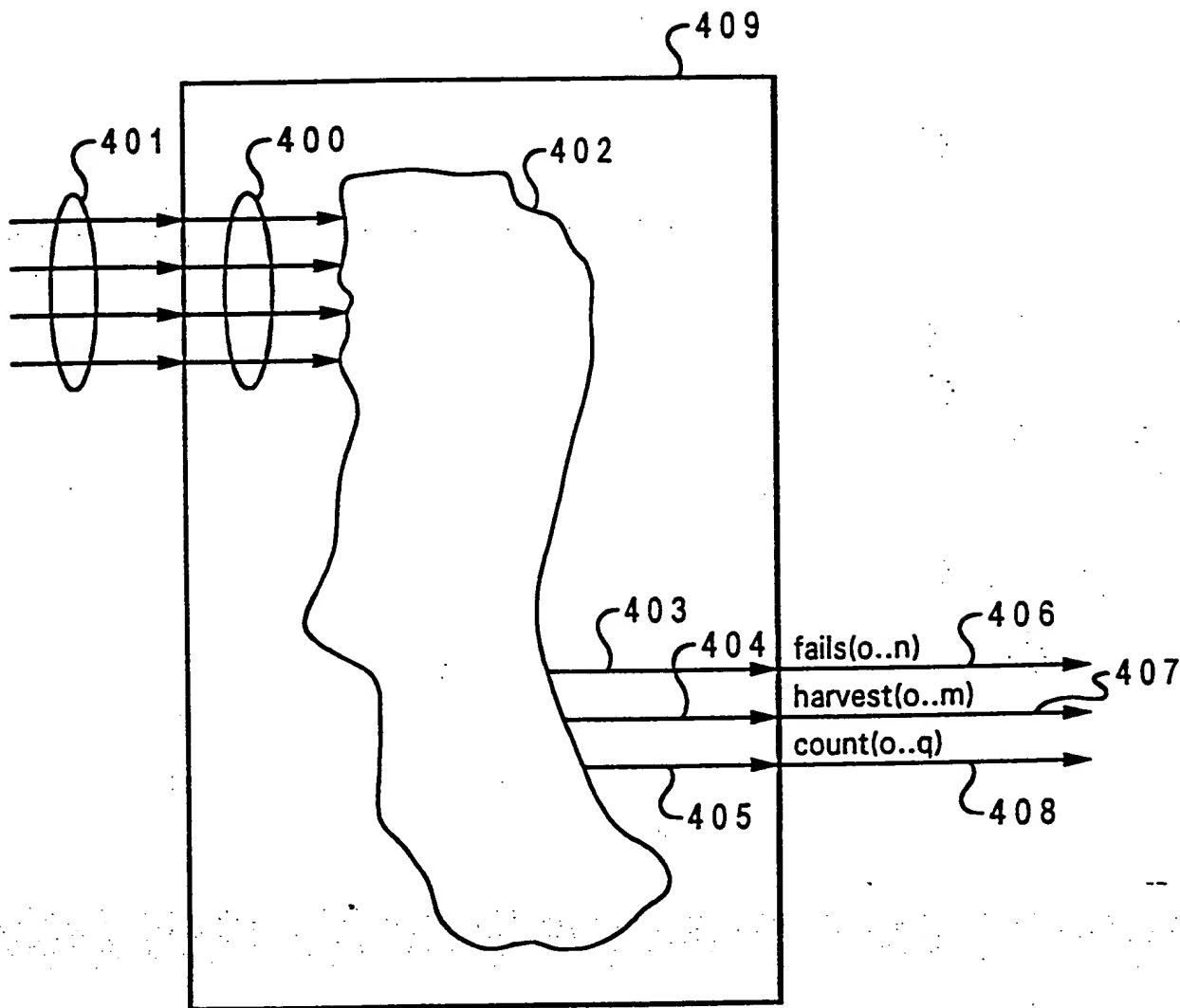


Fig. 4A

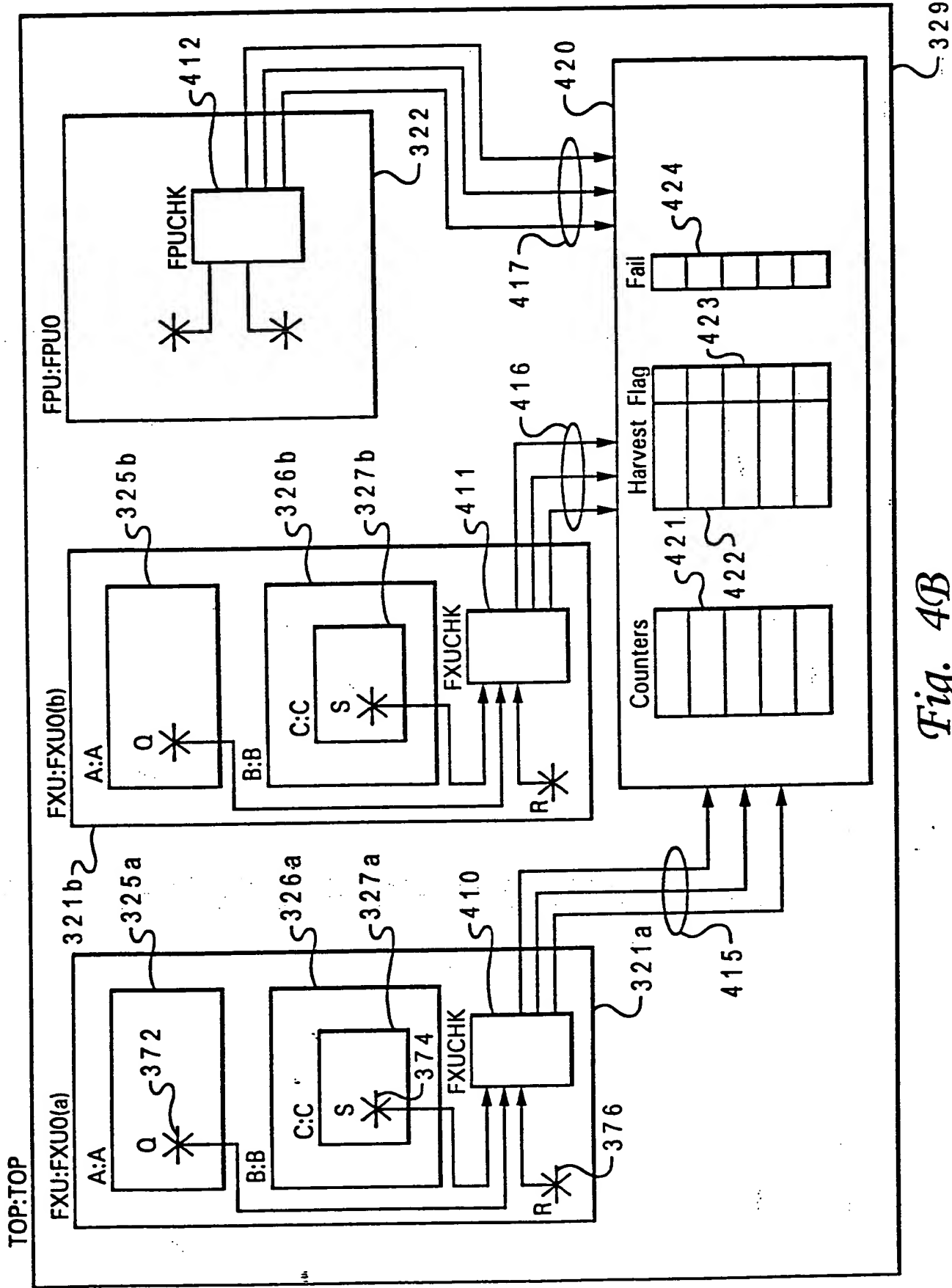


Fig. 4B

ENTITY FXUCHK IS

```

PORT(  S_IN      :    IN std_ulogic;
        Q_IN      :    IN std_ulogic;
        R_IN      :    IN std_ulogic;
        clock      :    IN std_ulogic;
        fails      :    OUT std_ulogic_vector(0 to 1);
        counts     :    OUT std_ulogic_vector(0 to 2);
        harvests   :    OUT std_ulogic_vector(0 to 1);
);

```

450

452 { --!! BEGIN
--!! Design Entity: FXU;

453 { --!! Inputs
--!! S_IN => B.C.S;
--!! Q_IN => A.Q;
--!! R_IN => R;
--!! CLOCK => clock;
--!! End Inputs

454 { --!! Fail Outputs;
--!! 0 : "Fail message for failure event 0";
--!! 1 : "Fail message for failure event 1";
--!! End Fail Outputs;

455 { --!! Count Outputs;
--!! 0 : <event0> clock;
--!! 1 : <event1> clock;
--!! 2 : <event2> clock;
--!! End Count Outputs;

456 { --!! Harvest Outputs;
--!! 0 : "Message for harvest event 0";
--!! 1 : "Message for harvest event 1";
--!! End Harvest Outputs;

457 { --!! End;

451

440

ARCHITECTURE example of FXUCHK IS

BEGIN

... HDL code for entity body section ...

END;

458

Fig. 4C

00622T" 208T5260

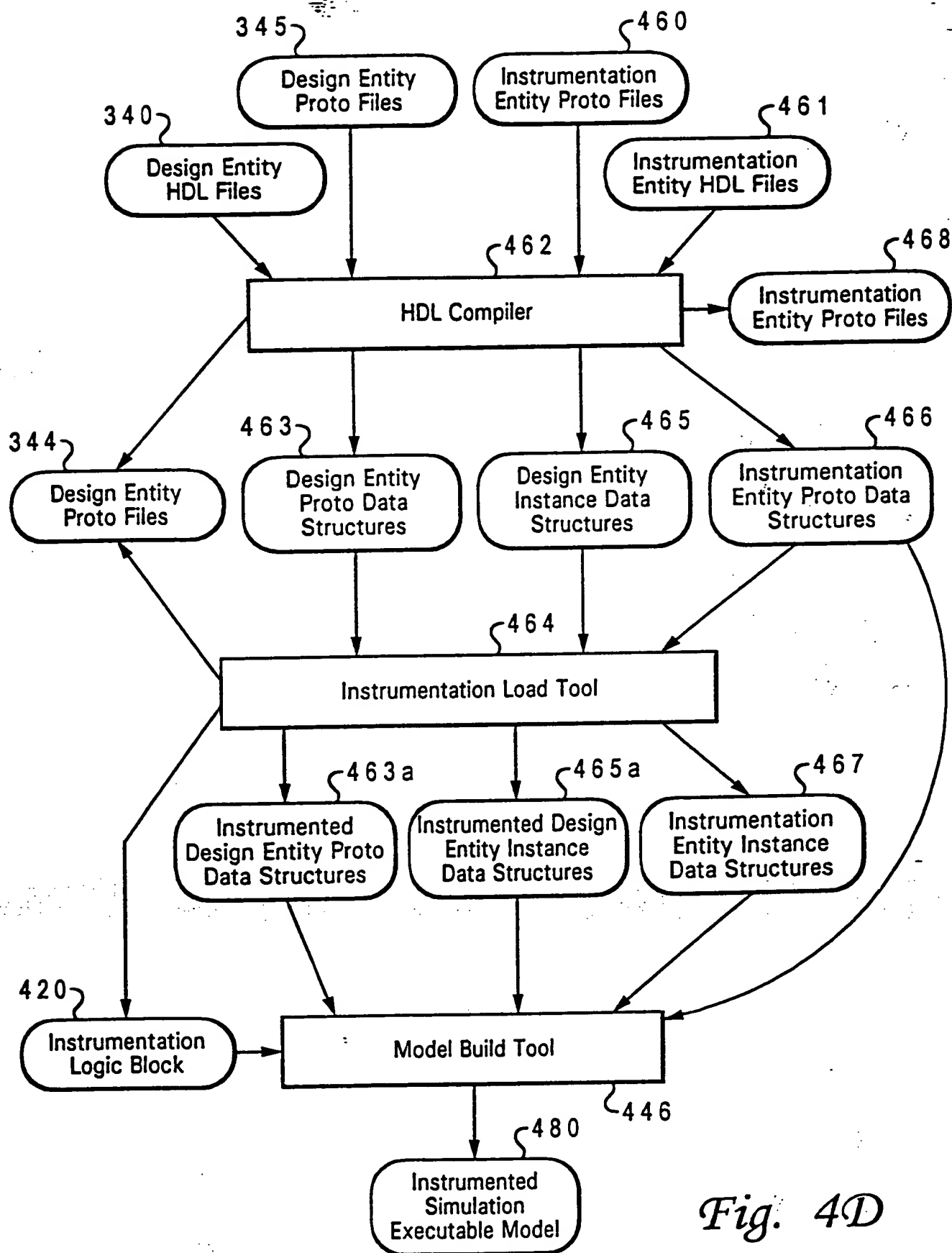


Fig. 4D

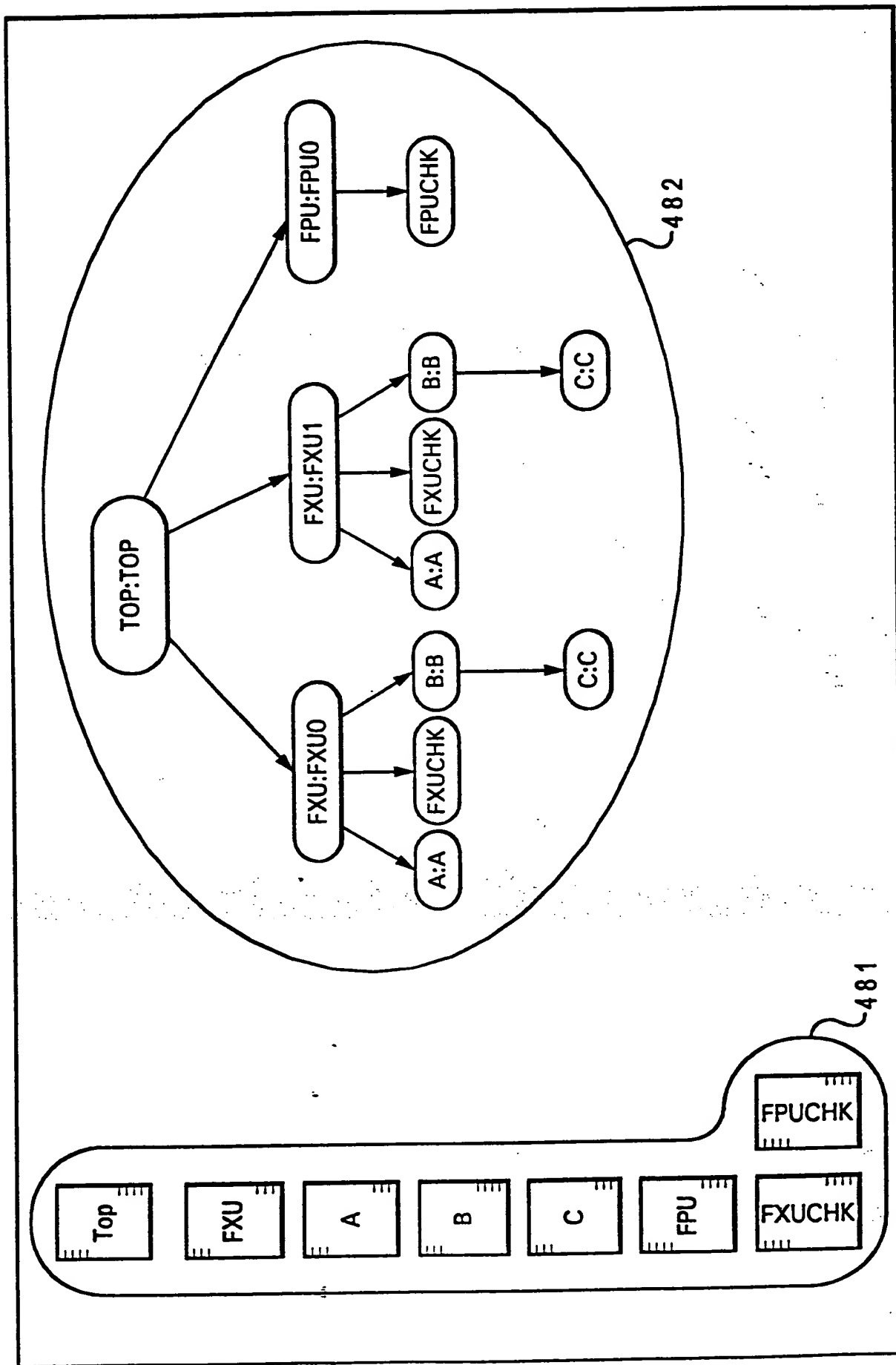


Fig. 4E

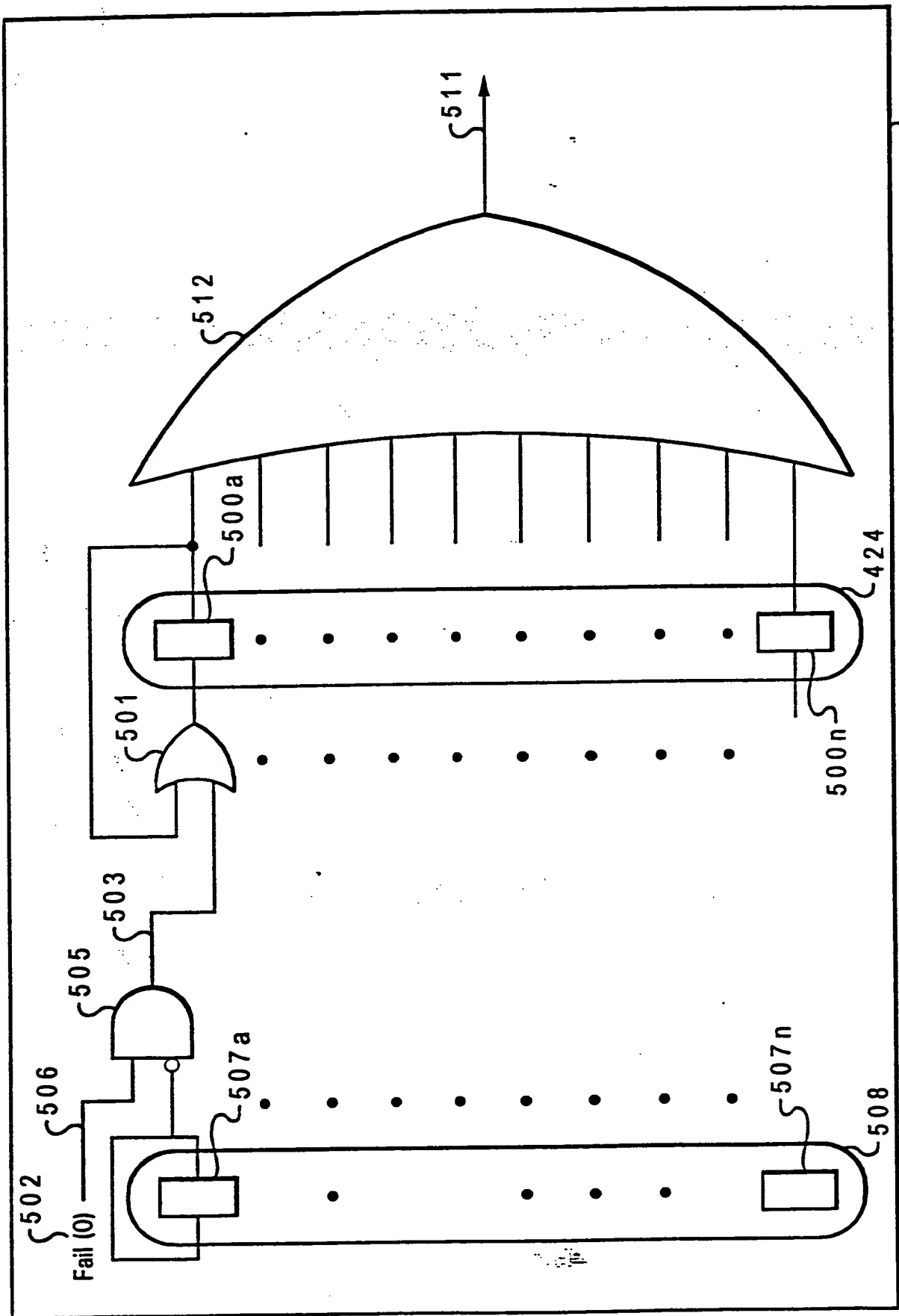


Fig. 5A

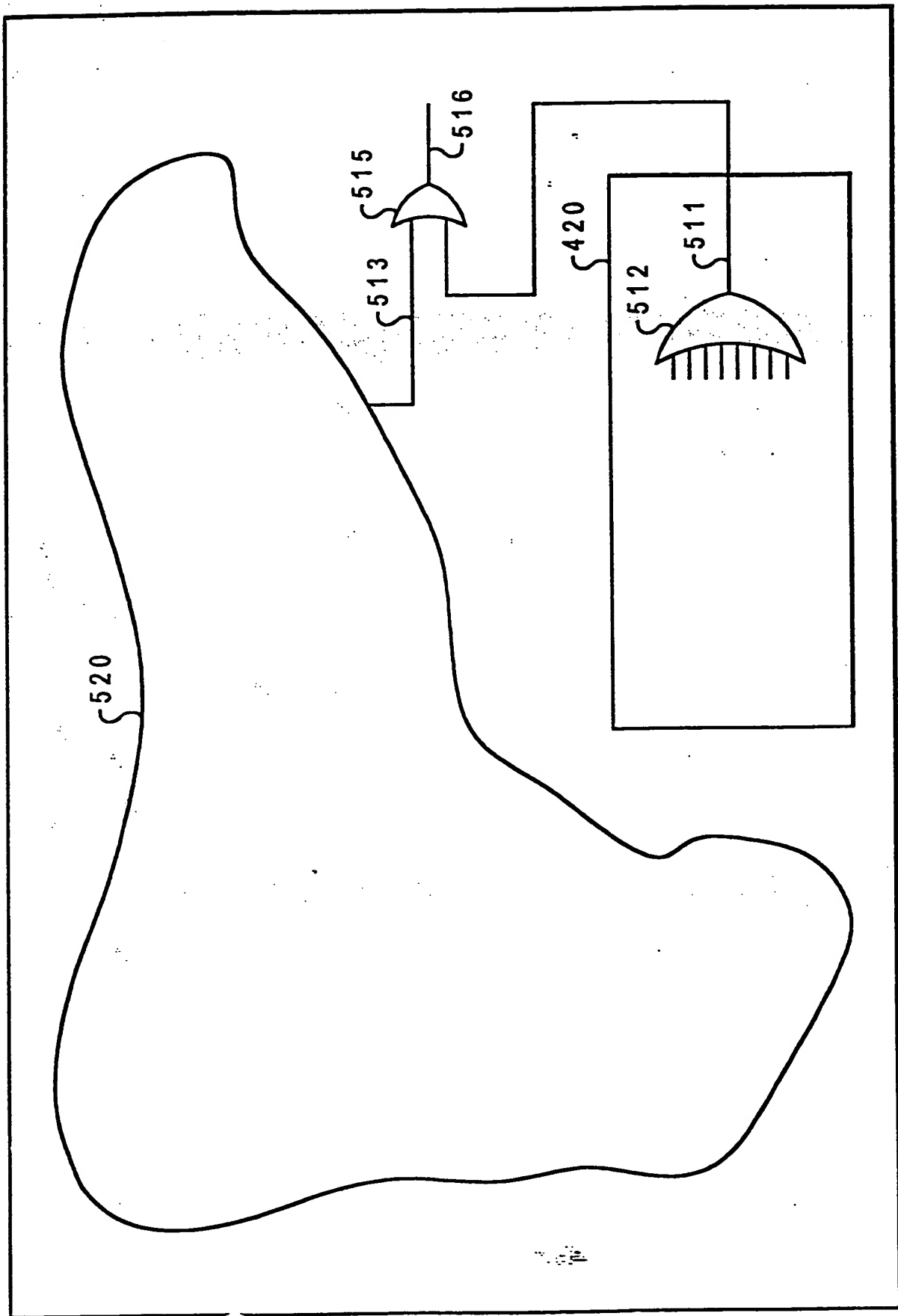


Fig. 5B

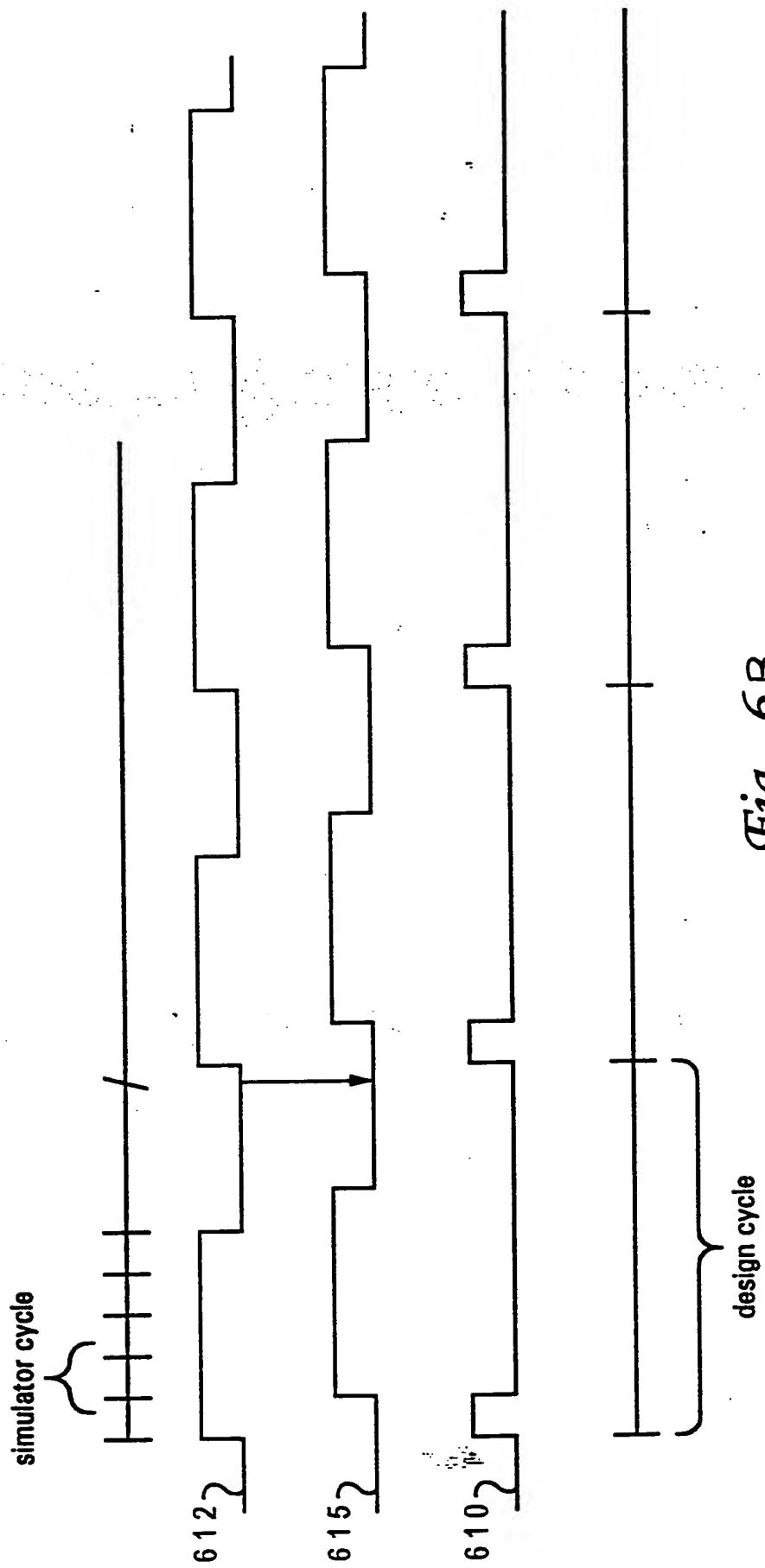


Fig. 6B

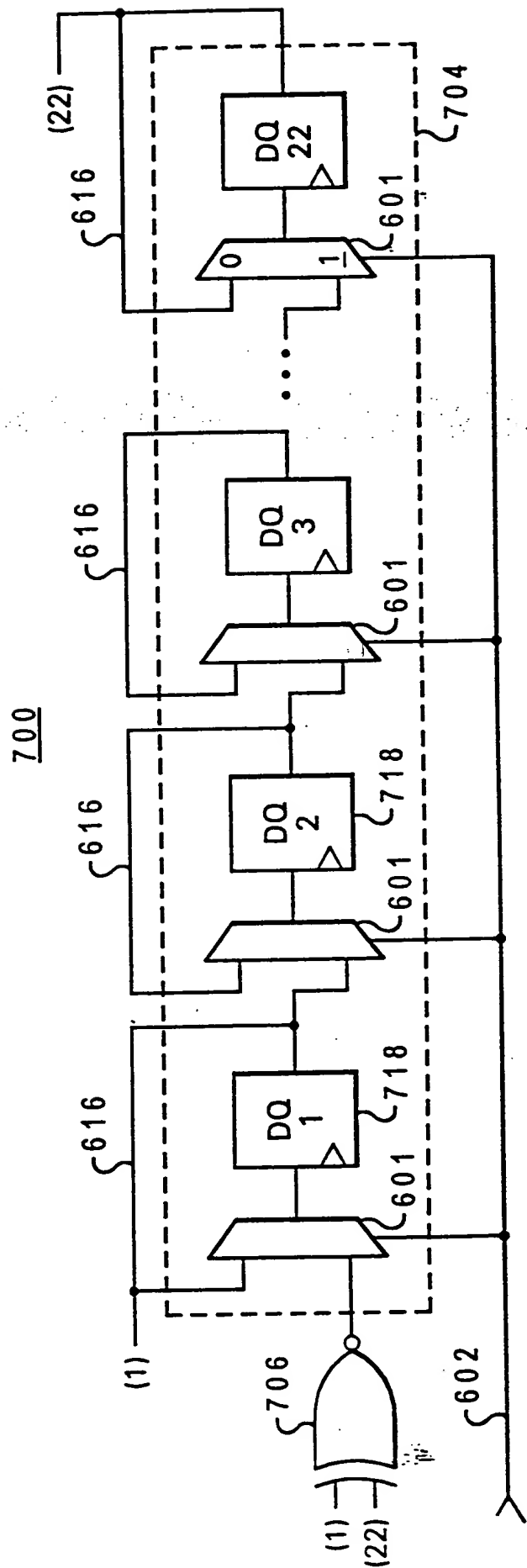


Fig. 7

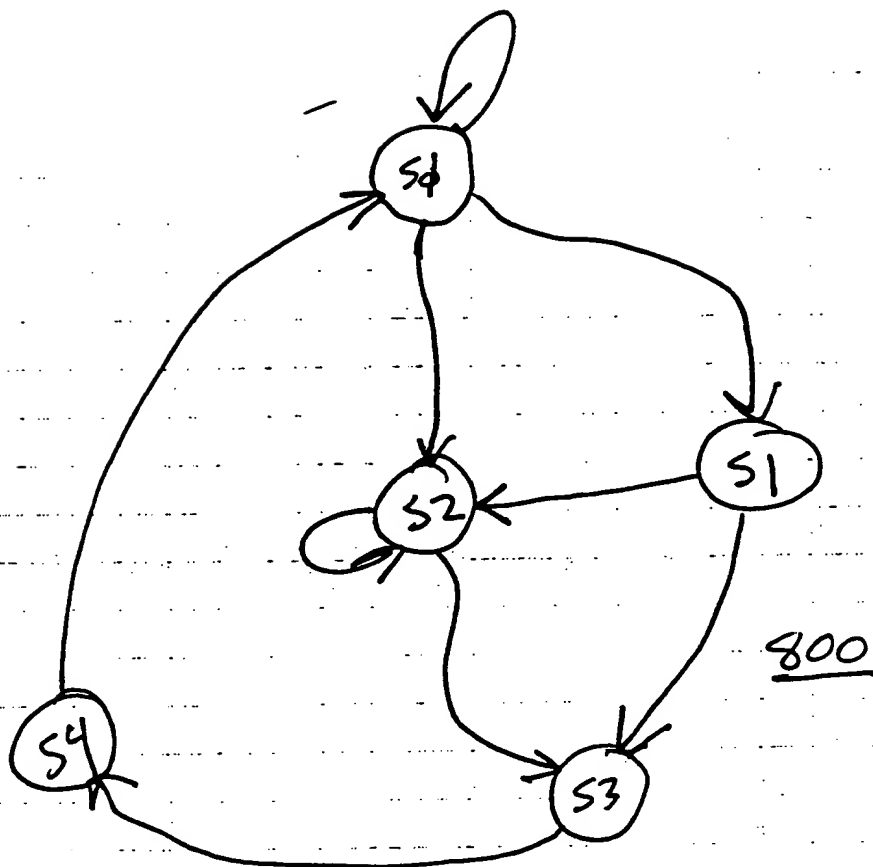


FIG. 8

(Prior Art)

entity Fsm: Fsm

850

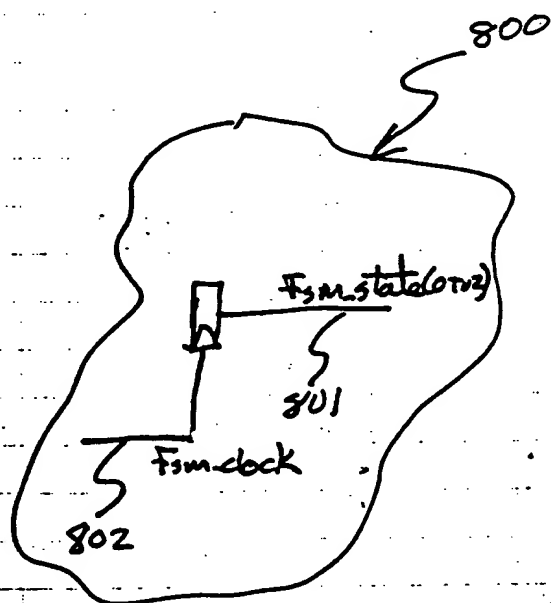


FIG. 8A
(Prior Art)

entity Fsm IS

PORT (

.... ports for entity Fsm

);

ARCHITECTURE Fsm of Fsm IS

BEGIN

.... HDL code for Fsm and rest of the entity. ...

fsm-state(0 to 2) <= ... signal 801

```
853 E --!! Embedded Fsm : exampleFsm;
859 E --!! clock          : (fsm_clock);
854 E --!! state_vector   : (fsm-state(0 to 2));
855 E --!! states vector    : (s0, s1, s2, s3, s4);
856 E --!! state_encoding : ('000', '001', '010', '011', '100');
857 E --!! arcs           : (s0 => s0, s0 => s1, s0 => s2,
                           s1 => s2, s1 => s3, s2 => s2,
                           s2 => s3, s3 => s4, s4 => s0);
858 E --!! end Fsm;
```

852

86

END;

FIG. 8B

entity FSM:FSM

850

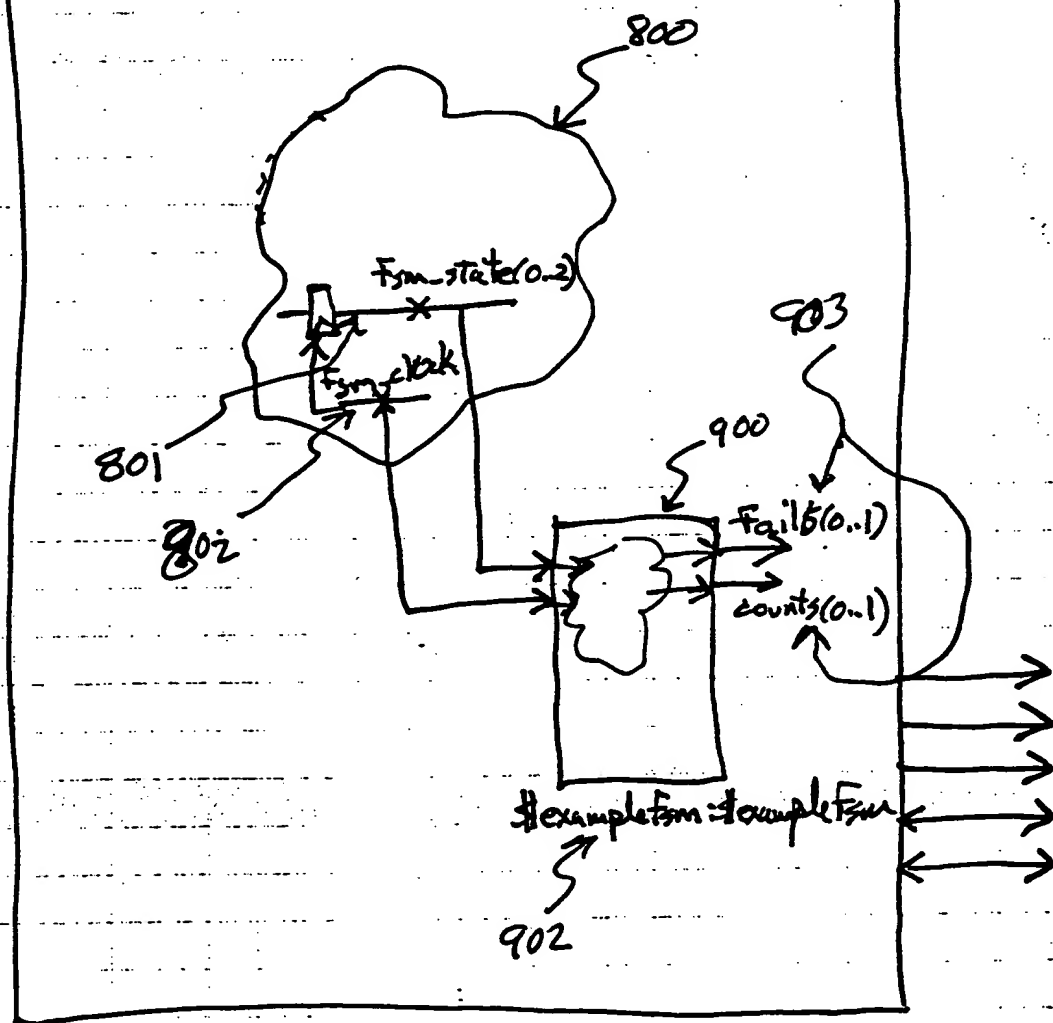


FIG. 9

[The page contains faint, illegible markings or bleed-through from the reverse side.]

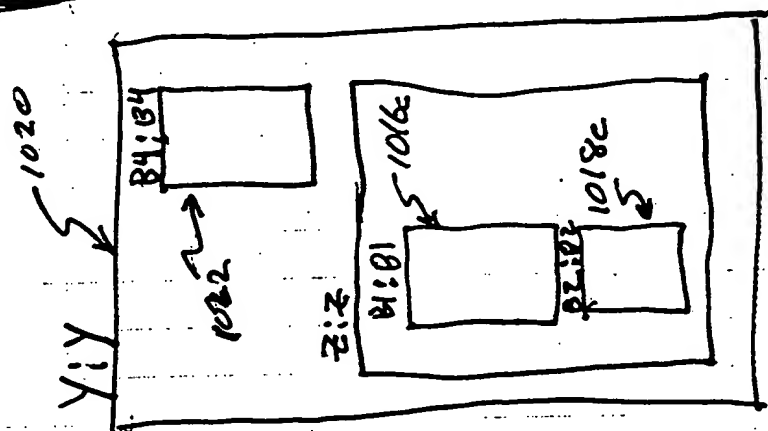
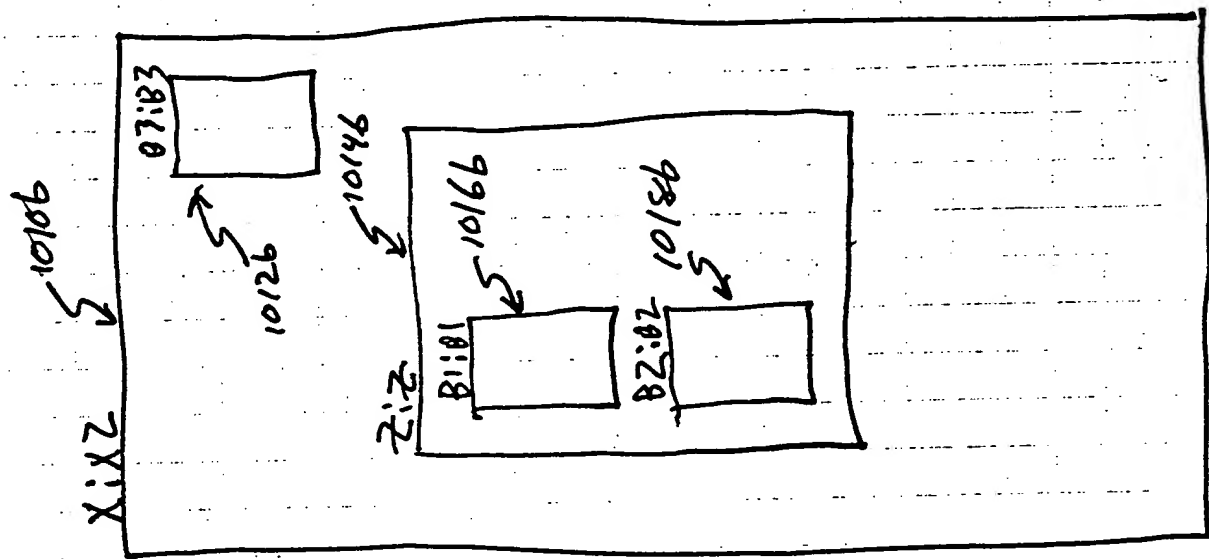
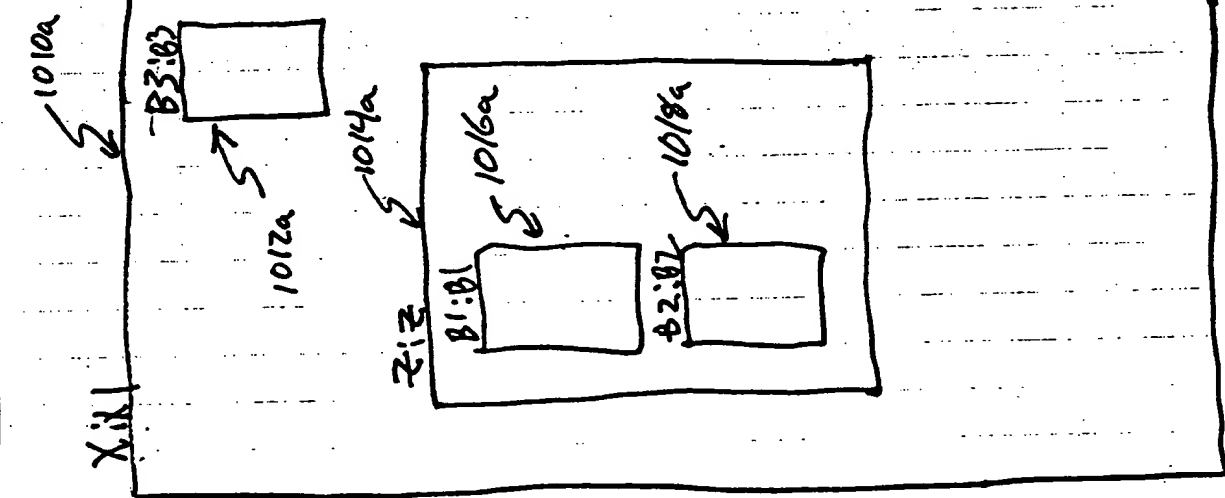


FIG. 10A

1030

1032

1034

1036

<instantiation identifier>, <instrumentation entity name>, <design entity name>, <event name>

FIG 10B

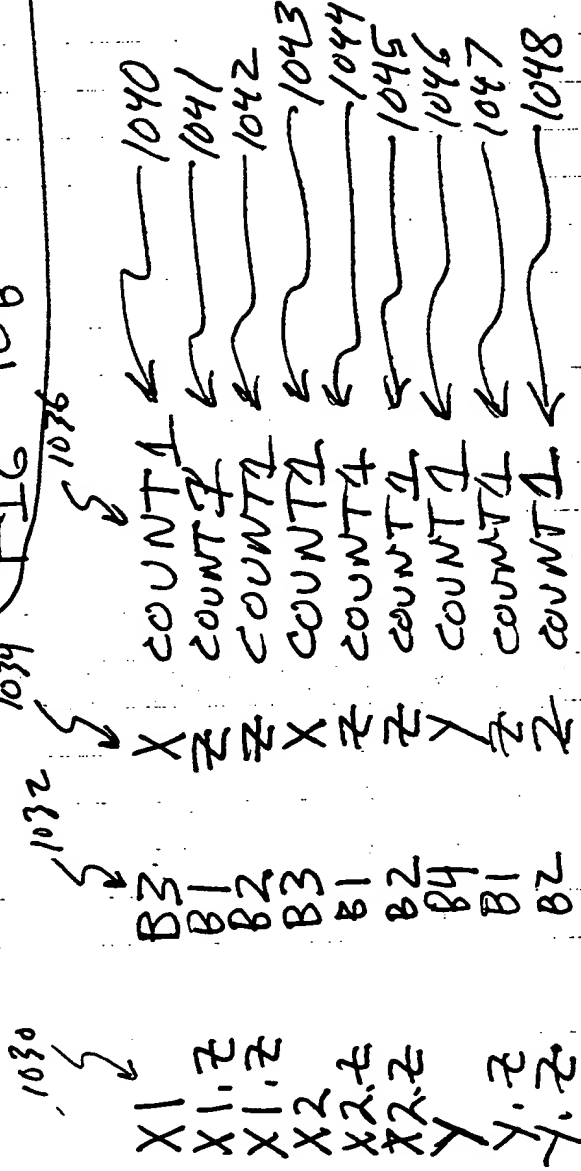


FIG 10C

